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PATTERSON & SHERIDAN, LLP
Gero McClellan / Qimonda
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056

EXAMINER	
BRITT, CYNTHIA H	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,025	RONZA ET AL.	
	Examiner	Art Unit	
	CYNTHIA BRITT	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-14,16,18-27,34,36 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-14,16,18-27,34,36 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/11/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/13/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-10, 12-14, 16, 18-27, 34, 36 and 37 are pending in the present application.

Response to Arguments

Applicant's arguments with respect to claims 1 and 16 have been considered but are moot in view of the new ground(s) of rejection.

However the examiner would like to point out that one of ordinary skill in the art may find a motivation to combine prior art references in the nature of the problem to be solved. **Ruiz v. A.B. Chance Co.,** 357 F.3d 1270, 1276, 69 USPQ2d 1686, 1690 (Fed. Cir. 2004); Also **Pro-Mold & Tool Co. v. Great Lake Plastic Inc.**, 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630; **In re Huang**, 100 F.3d 135, 139 n.5; 40 USPQ2d 1685, 1688 n.5 (Fed. Cir. 1996). Each of the prior art references are directed to testing and repairing/replacing failed memory elements using row/column/word/bit replacement.

Further, where a claimed improvement on a device or apparatus is no more than "the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement," the claim is unpatentable under 35 U.S.C. 103(a). Ex Parte Smith, 83 USPQ.2d 1509, 1518-19 (BPAI, 2007) (citing KSR v. Teleflex, 127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)). The claimed invention only unites old elements by combining the type of replacements being preformed (row/column/word) with no change in the respective functions of those old elements, and the combination of those elements yields predictable results. Accordingly, since the applicant[s] have submitted no persuasive

evidence that the combination of the above elements is uniquely challenging or difficult for one of ordinary skill in the art, and it is no more than the predictable use of prior art elements according to their established functions resulting in the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 16, 34, 36, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al. U.S. Patent No. 5,161,157 in view of Applicant's admitted prior art., and further in view of Eustis et al. U.S. Patent No. 6,928,377.

As per claims 1, 16, 34, 36, and 37 Owen et al. teach a circuit and method for detecting defective storage cells; replacing at least one of a row or column containing one or more defective storage cells with a redundant row or column; and replacing at least one word containing one or more defective storage cells with a redundant word without replacing the entire row containing the at least one word (column 5 lines 21-40 and 46-51). Owen et al. also teach a register for storing an address of a current row under test; a register for storing a number of faults in a current row under test; a plurality of n row address registers for storing addresses of rows having defective storage cells; and a plurality of n fault count registers for storing a corresponding number of faults in each row having an address stored in a row address register (column 5 lines 21-40 and 46-51, column 11 line 66 through column 12 line 13, Figure 5 – also see the independent claims with the following definition). *The term memory cells refers to a particular grouping of data bits, such as data bits, data words, array rows, or array columns. (Column 1 lines 35-37)

Further, the present specification states:

[0007] Classical repair strategies consist of replacing rows or columns for which at least one cell is defective. This simple criteria leads to excess waste of spare cells

whenever the number of faulty cells in one row/column is significantly less than the total cells replaced.

[0008] New repair strategies are able to repair small groups of logically neighboring cells (memory words) instead of complete rows and columns. Such word replacement is more flexible than row and column replacement in that it allows fixing sparse faulty cells, but it is not suitable for repairing column or periphery defects and, to some extent, row defects. Repair algorithms are not necessary for this type of redundancy, as words are replaced at testing run time after detection of faults.

Not explicitly disclosed by AAPA and Owen et al. is; overwriting stored addresses of one of columns and rows having a first number of defective storage cells with addresses of one of columns and rows having a second number of defective storage cells, wherein the second number is greater than the first number. However, in an analogous art, Eustis et al. (column 4 lines 35-45) teaches overwriting stored addresses of one of columns and rows having a first number of defective storage cells with addresses of one of columns and rows having a second number of defective storage cells, wherein the second number is greater than the first number. Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used a combination of the prior art memory test/repair methods in order to effectively use the redundant memories. (see Ex Parte Smith, 83 USPQ.2d 1509, 1518-19 (BPAI, 2007) (citing KSR v. Teleflex, 127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)). Accordingly as the claimed invention only unites old elements with no change in the respective functions of those old elements, and the combination of

those elements yields predictable results; absent evidence that the modifications necessary to effect the combination of elements is uniquely challenging or difficult for one of ordinary skill in the art, the claimed invention would be obvious.

Claims 1- 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,862,703, Oonk in view of Deas U.S. Patent No. 6,065,090 and further in view of Eustis et al. U.S. Patent No. 6,928,377.

As per claim 1, Oonk substantially teaches a memory tester in accordance with the invention tests a random access memory device under test (DUT) comprising an array of rows and columns of memory cells, each having a separate row and column address. The tester provides a computer with enough information to determine how to efficiently allocate spare rows and columns for replacing rows and columns containing defective memory cells. As the tester tests each memory cell residing at a particular address within the DUTs, it writes a fail data bit into a corresponding address of an error capture memory (ECM) to indicate whether the memory cell is defective (column 2 lines 37-48). Not disclosed is the selective replacement of failed memory words, rows, and columns.

However, in an analogous art, Deas teaches the bits chosen for each defective location can be different for each slice. If there were a column error in one of the blocks then it would be preferable to use the full column address and a curtailed row address rather than the fill row address and a curtailed column address. Both of these options (full row--partial column, and partial row--fill column) may be used. (Column 2 lines 46-53, Column 3 lines 8-24) Therefore, it would have been obvious to a person having

ordinary skill in the art at the time this invention was made to have used the selective replacement of failed memory words, rows, and columns as taught by Deas with the tester of Oonk.

Not explicitly disclosed by Oonk and Deas et al. is; overwriting stored addresses of one of columns and rows having a first number of defective storage cells with addresses of one of columns and rows having a second number of defective storage cells, wherein the second number is greater than the first number. However, in an analogous art, Eustis et al. (column 4 lines 35-45) teaches overwriting stored addresses of one of columns and rows having a first number of defective storage cells with addresses of one of columns and rows having a second number of defective storage cells, wherein the second number is greater than the first number. Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used a combination of the prior art memory test/repair methods in order to effectively use the redundant memories. (see Ex Parte Smith, 83 USPQ.2d 1509, 1518-19 (BPAI, 2007) (citing KSR v. Teleflex, 127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)). Accordingly as the claimed invention only unites old elements with no change in the respective functions of those old elements, and the combination of those elements yields predictable results; absent evidence that the modifications necessary to effect the combination of elements is uniquely challenging or difficult for one of ordinary skill in the art, the claimed invention would be obvious.

As per claim 2, Oonk teaches the computer reads the counts in one or more of the area fail counters when the test is completed to determine whether the DUT has any

defective cells, and if so, which areas of the DUT's memory space contain the defective cells. In some cases, the computer will be able to determine whether and how to allocate spare rows and columns to replace DUT rows and columns containing defective memory cells on the basis of the count data alone. (Column 2 lines 49-63)

As per claim 3, Oonk teaches allocating a redundant row or column to a first row or column containing defective storage cells in preference over a second row or column containing a lesser number of defective storage cells. (Column 2 lines 55-63)

As per claim 4, Oonk teaches replacing the defective storage cells of the second row or column with one or more redundant words. (Column 6 lines 29-59)

As per claim 5, Oonk teaches one redundant word replaces defective storage cells of at least two columns. (Column 7 lines 19-30)

As per claim 6, Oonk teaches activating a FAIL signal to indicate the memory device is not repairable if all defective cells detected cannot be replaced. (Column 5 lines 35-60)

As per claims 7, 9, and 13, Oonk teaches a memory tester in accordance with the invention tests a random access memory device under test (DUT) comprising an array of rows and columns of memory cells, each having a separate row and column address. The tester provides a computer with enough information to determine how to efficiently allocate spare rows and columns for replacing rows and columns containing defective memory cells. As the tester tests each memory cell residing at a particular address within the DUTs, it writes a fail data bit into a corresponding address of an error capture memory (ECM) to indicate whether the memory cell is defective (column 2 lines

37-48). Not disclosed by Oonk is that the method is preformed by a BIST and that a specific Row or Column test is preformed. However, AAPA discloses prior art methods which teach all of the above (AAPA [0012-0014]) Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the above methods with the method of Oonk in order to provide a test and repair method on chip. Accordingly, since the applicant[s] have submitted no persuasive evidence that the combination of the above elements is uniquely challenging or difficult for one of ordinary skill in the art, the claim is unpatentable as obvious under 35 U.S.C. 103(a) because it is no more than the predictable use of prior art elements according to their established functions resulting in the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement.

As per claim 7,AAPA teaches the method is performed as part of a built-in self test (BIST) of the memory device. AAPA [0012]

As per claim 8, AAPA teaches the BIST serves multiple memory devices with embedded and shared redundant elements. AAPA [0012]

As per claim 9, AAPA teaches detecting defective storage cells comprises conducting a column test. AAPA [0012]

As per claim 10, AAPA teaches, wherein conducting the column test comprises identifying and storing addresses of columns having greater than a threshold number of defective storage cells. AAPA [0012-0014]

As per claim 12, AAPA teaches detecting defective storage cells comprises conducting a row test. AAPA [0012]

As per claim 13, AAPA teaches detecting defective storage cells comprises conducting a row test. AAPA [0012]

As per claim 14, Oonk teaches conducting the row test comprises identifying and storing addresses of rows having greater than a threshold number of defective storage cells. AAPA [0012-0014]

Claims16, 18-21, 23-25, 27, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,795,942 Schwartz in view of Deas U.S. Patent No. 6,065,090 and further in view of Eustis et al. U.S. Patent No. 6,928,377.

As per claims 16 and 34, Schwartz teaches a self-repairing memory device comprising: at least one array of storage cells arranged in columns and rows, with each row comprising multiple words; at least one of redundant row or column elements for replacing rows or columns containing defective storage cells; and at least one block of redundant word elements for replacing words containing defective storage elements without replacing the entire rows containing the words being replaced. (Column 2 line 42 through column 3 line 3) Not explicitly taught by Schwartz is the selective replacement of failed memory words, rows, and columns.

However, in an analogous art, Deas teaches the bits chosen for each defective location can be different for each slice. If there were a column error in one of the blocks then it would be preferable to use the full column address and a curtailed row address

rather than the fill row address and a curtailed column address. Both of these options (full row--partial column, and partial row--fill column) may be used. (Column 2 lines 46-53, Column 3 lines 8-24) Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the selective replacement of failed memory words, rows, and columns as taught by Deas with the memory device of Schwartz.

Not explicitly disclosed by Schwartz and Deas et al. is; overwriting stored addresses of one of columns and rows having a first number of defective storage cells with addresses of one of columns and rows having a second number of defective storage cells, wherein the second number is greater than the first number. However, in an analogous art, Eustis et al. (column 4 lines 35-45) teaches overwriting stored addresses of one of columns and rows having a first number of defective storage cells with addresses of one of columns and rows having a second number of defective storage cells, wherein the second number is greater than the first number. Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used a combination of the prior art memory test/repair methods in order to effectively use the redundant memories. (see Ex Parte Smith, 83 USPQ.2d 1509, 1518-19 (BPAI, 2007) (citing KSR v. Teleflex, 127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)). Accordingly as the claimed invention only unites old elements with no change in the respective functions of those old elements, and the combination of those elements yields predictable results; absent evidence that the

modifications necessary to effect the combination of elements is uniquely challenging or difficult for one of ordinary skill in the art, the claimed invention would be obvious.

As per claim 18, Schwartz teaches the built-in self repair (BISR) circuitry is configured to allocate redundant row or column elements to rows or columns containing defective storage cells based on the number of defective storage cells contained therein. (Column 2 line 42 through column 3 line 3)

As per claim 19, Schwartz teaches the built-in self repair (BISR) circuitry is configured to replace, with redundant word elements, defective storage cells contained in rows or columns not allocated redundant row or column elements. (Column 2 line 42 through column 3 line 3)

As per claim 20, Schwartz teaches: the at least one array of storage cells comprises multiple arrays of storage cells; and at least two of the arrays of storage cells share the block of redundant word elements. (Column 2 line 42 through column 3 line 3)

As per claim 21, Schwartz teaches the at least one array of storage cells comprises multiple arrays of storage cells; the at least one of redundant row or column elements for replacing rows or columns containing defective storage cells comprises redundant row elements and redundant column elements; and each array of storage cells is provided with at least one BISR circuit. (Column 2 line 42 through column 3 line 3)

As per claim 23, Schwartz teaches the built-in self repair (BISR) circuitry comprises: row test circuitry; and a plurality of registers to store address of rows

containing at least a first threshold number of defective memory cells, as detected by the row test circuitry. (Column 2 line 42 through column 3 line 3)

As per claim 24, Schwartz teaches the built-in self repair (BISR) circuitry further comprises: column test circuitry; and a plurality of registers to store address of columns containing at least a second threshold number of defective memory cells, as detected by the row test circuitry. (Column 2 line 42 through column 3 line 3)

As per claim 25, Schwartz teaches the built-in self repair (BISR) circuitry comprises: column test circuitry; and a plurality of registers to store address of columns containing at least a threshold number of defective memory cells, as detected by the column test circuitry. (Column 2 line 42 through column 3 line 3)

As per claim 27, Schwartz teaches a memory built-in self test (BIST) circuit to identify defective storage cells. (Column 2 line 42 through column 3 line 3)

Claims 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,795,942 Schwartz.

As per claims 22 and 26,Schwartz substantially teaches the claimed self-repairing memory device comprising: at least one array of storage cells arranged in columns and rows, with each row comprising multiple words; at least one of redundant row or column elements for replacing rows or columns containing defective storage cells; and at least one block of redundant word elements for replacing words containing defective storage elements without replacing the entire rows containing the words being replaced. (Column 2 line 42 through column 3 line 3) not disclosed by Schwartz is that the storage cells are dynamic storage cells and/or that the "bank of *non-volatile* storage

elements to store addresses of at least one of rows or columns to be replaced with redundant rows or columns". However the examiner would like to point out that these specific types of memory would be merely a design choice as both nonvolatile memory and dynamic memory are well known in the art for these purposes. Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used this type of memory.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See form 892 attached.

The examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider each of the cited references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage disclosed by the examiner.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CYNTHIA BRITT whose telephone number is (571)272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Cynthia Britt/
Primary Examiner, Art Unit 2117